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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/505,382	02/16/2000	Roy R. Faget	10001840-1	6474

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EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

DATE MAILED: 02/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/505,382	Applicant(s) FAGET, ROY R.	
	Examiner Chat C. Do	Art Unit 2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *2/16/00* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-7, 9-17, and 19-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Tanihira et al. (U.S. 5,553,010).

Re claims 1, 7, 9, 11, 17, and 19, Tanihira et al. disclose a logic circuit in Figure 6 for shifting the input data (Din). The logic circuit comprises a plurality of logic gates (Logic I 110-113 & 15, Logic II 120-123 & 16, Logic III 130-133 & 17, Logic IV 140-143 & 18) for receiving data input (Din0-Din3) and control signals (S0-S3 and 19) wherein each data input uses a single transistor (each input goes to a single transistor of an AND gate); and a plurality of shared data lines (Din0-Din2 bus) connecting logic gates. The shared data lines (Din0-Din2 bus) interfacing through a transistor on each of the logic gates (above Logic I-IV gates) to provide a portion of the data inputs (Din0-Din2) for each of the logic gates by connecting data inputs among the plurality of logic gates. The logic gates shift data received at the data inputs by one data bits based upon the control signals (S0-S3 and 19) and the connections of the shared data lines (Din0-Din2 bus) wherein each of the logic gates receives one data input (Din 3) using the single transistor for the data input and receives other data inputs (Din0-Din2) from the plurality

of shared data lines (Din0-Din2 bus). In addition, Tanihira et al. disclose the logic gate in Figure 6 shift data received at the data inputs (Din) based upon the control signals (S0-S3) and connections of the shared data. Tanihira et al. disclose the first and second control signals are enable to shift either left/right (output data).

Re claims 2 and 12, Tanihira et al. disclose the above logic circuit in Figure 26 wherein each of the logic gates includes first (34 and 35) and second (20) stages shift operation.

Re claims 3 and 13, Tanihira et al. disclose the above logic circuit in Figure 26 wherein each of the logic gates includes two set of control signal (first and second specification signals), one for first stage and one for second stage.

Re claims 4 and 14, Tanihira et al. disclose the above logic circuit comprising another plurality of shared data lines (output 344 and 354) for providing data inputs to the second stage shifting operation.

Re claims 5 and 15, Tanihira et al. disclose the above logic circuit in Figure 6 wherein the plurality of shared data lines connect adjacent logic gates (Din bus) among the plurality of logic gates.

Re claims 6 and 16, Tanihira et al. disclose the above logic circuit in Figure 6 wherein each of the logic gates receives one of the data inputs (Din) as a primary data line.

Re claims 10 and 20, Tanihira et al. disclose the above logic circuit in Figure 6 wherein each of the shared data lines connect one of the logic gates with a plurality of the logic gates.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being obvious over Tanihira et al. (U.S. 5,553,010) in view of Wong et al. (U.S. 5,822,231).

Re claims 8 and 18, Tanihira et al. disclose the above logic circuit in Figure 6 wherein each of the logic gates control by the control signals (S0-S3). Tanihira et al. does not disclose the logic gates including a plurality of transistors. However, Wong et al. disclose in Figure 2 the logic gates compose of a plurality of transistors. Therefore, it would have been obvious to a person having ordinary skill in the art to include a plurality of transistors in the logic gates for controlling the logic signal because it would enable to control the logic signal.

Response to Arguments

5. Applicant's arguments filed January 16, 2003 have been fully considered but they are not persuasive.

The applicant argues in the independent claim 1 as the apparatus and the independent claim 11 as the method that the cited reference, Tanihira et al. (U.S. 5,553,010), does not disclose or suggest "wherein each data input uses a single

transistor...the shared data lines interfacing through a transistor on each of the logic gates to provides a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates,...wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines" in the last and second paragraphs in pages 4 and 5.

It is respectfully submitted that although Tanihira et al. (U.S. 5,553,010) does not explicitly show a transistor receiving an input data, It is well known in the art that an AND gates are structured by transistors, and an input received by an AND gate as shown by Tanihira et al. must goes through a transistor as claimed. Therefore, the recited reference by Tanihira et al. (U.S. 5,553,010) disclose the cited limitation in claims 1 and 11.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (703) 305-5655. The examiner can normally be reached on M => F from 7:00 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (703) 305-9662. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Chat C. Do
Examiner
Art Unit 2124

January 28, 2003

CHUONG DINH NGO
PRIMARY EXAMINER